
Time-Based ADC and TDC Architectures

Abdel Yousif and Jim Haslett
University of Calgary

Agenda

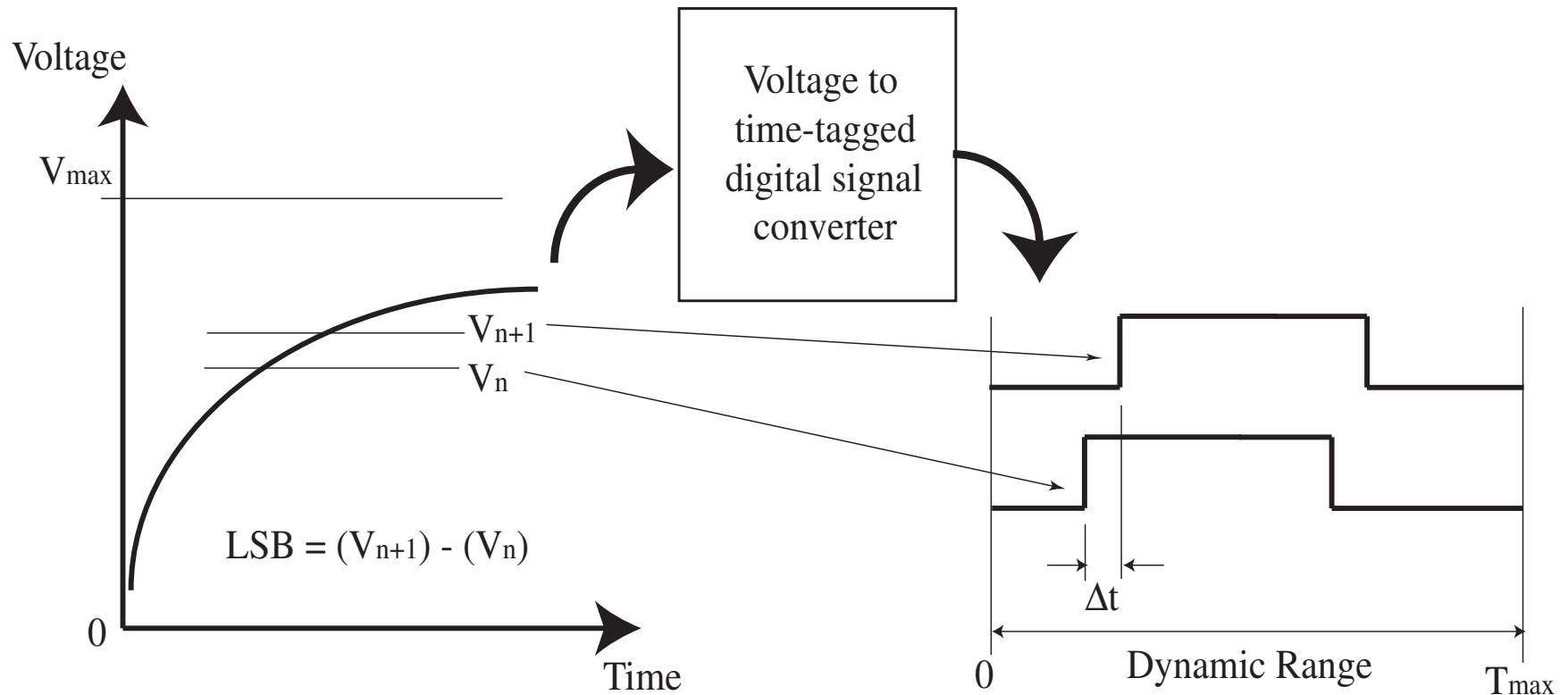
- Background: time-based data processing
- Design components and applications
- PET imaging application
- TDC architecture
- ADC architecture
- Conclusions

Background

“In a submicron CMOS process (90nm and beyond), time-domain resolution of a digital signal edge transition is superior to voltage resolution of an analog signal”

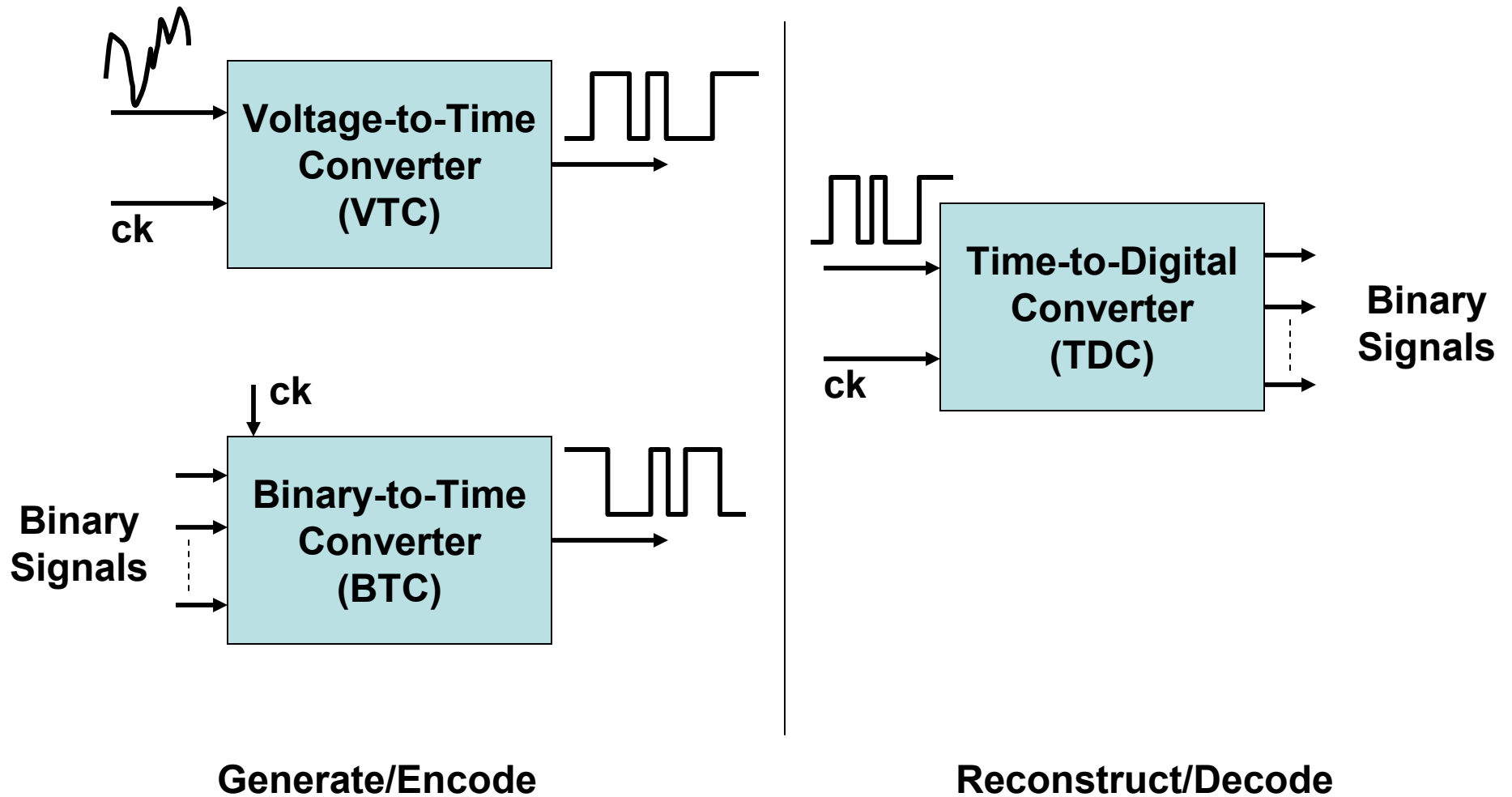
Robert (Bogdan) Staszewski, TI

Time-Based Data Processing

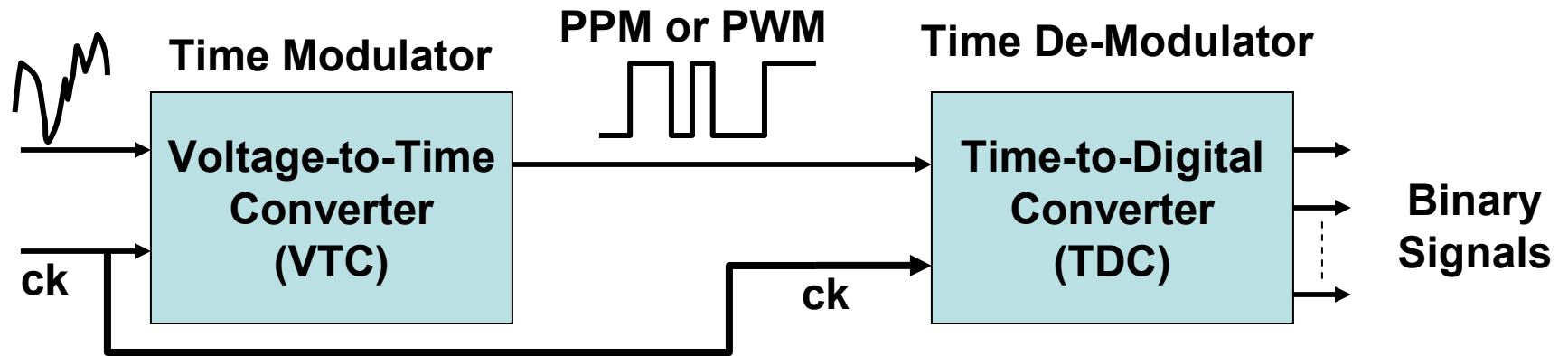


Process Scaling

Time Processing: Design Components

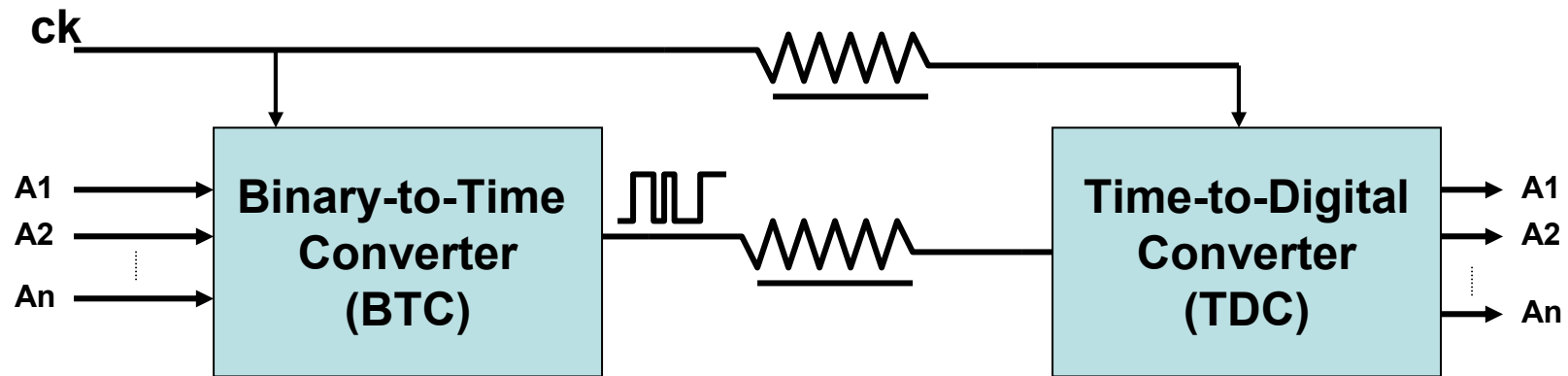


Applications: ADC Architecture



- Low power and high speed architecture
- Bit resolution is scalable with process
- Optimized for multi-channel performance

Applications: Serial Links



- On-chip and Off-chip data links
- Data rate linked to highest delay resolution
- Signaling techniques to guarantee signal integrity and PVT control

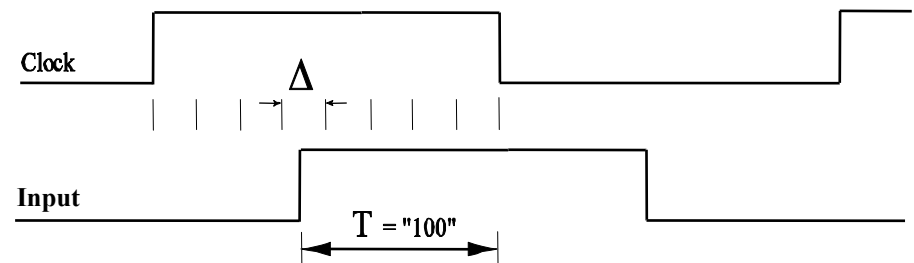
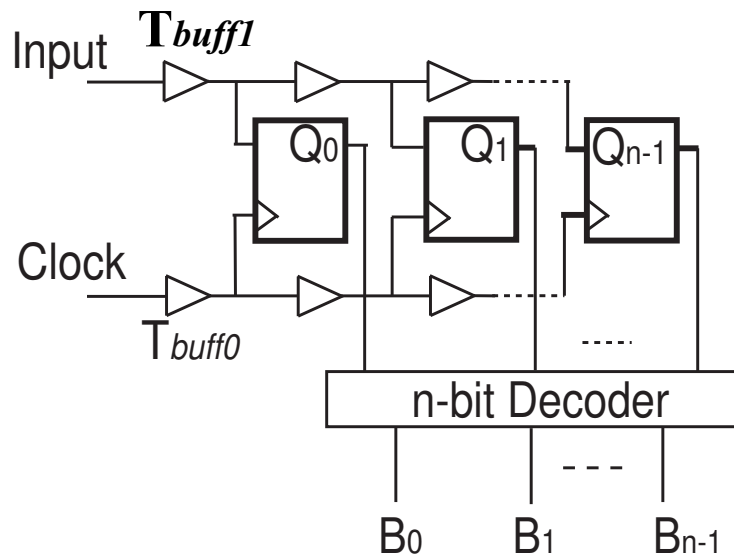
Applications: TDC for PET Imaging

- Positron Emission Tomography (PET) is a nuclear medicine imaging technique



A Traditional TDC Architecture

- A Time to Digital Converter (TDC) measures the time difference between two signal edges/events



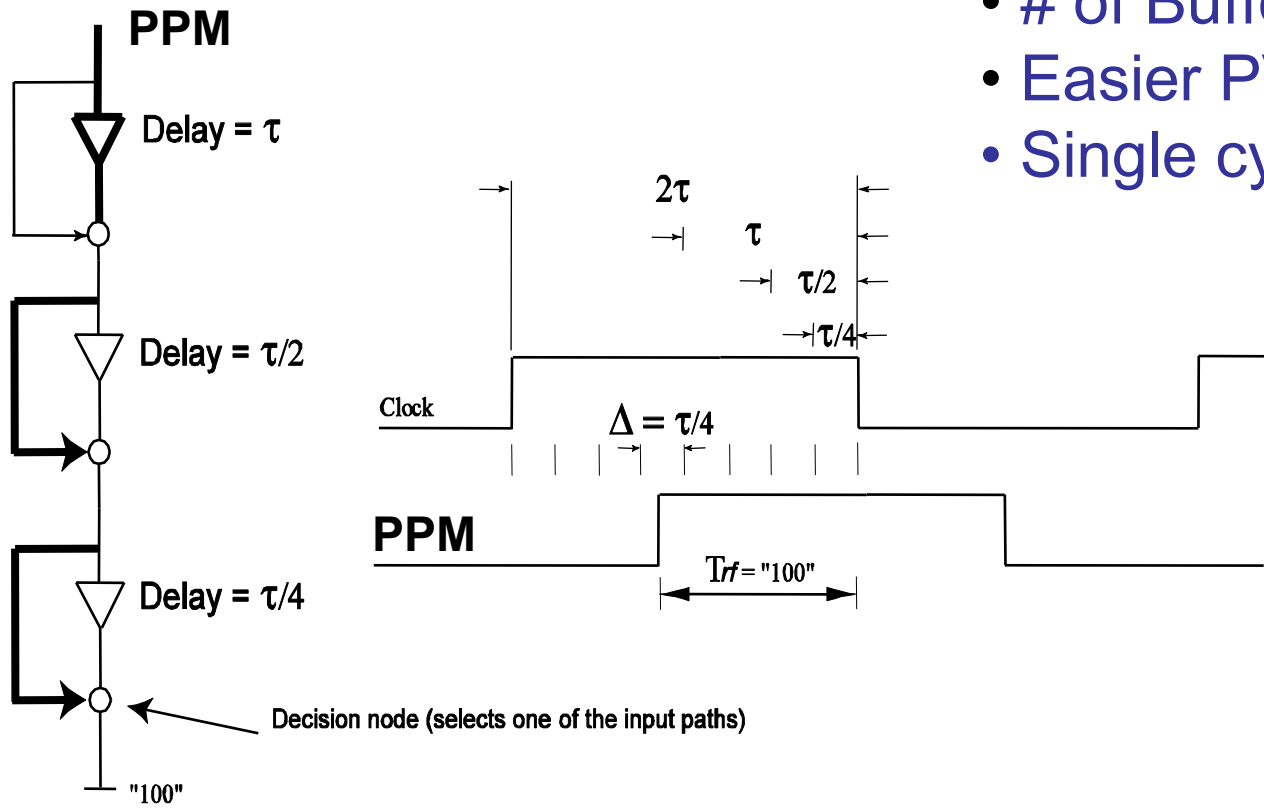
$$\# \text{ of Buffers} = 2(2^n - 1)$$

$$\text{Time resolution, } \Delta = T_{buff1} - T_{buff0}$$

- Differential signaling
- Multi-cycle operation
- Limited dynamic range

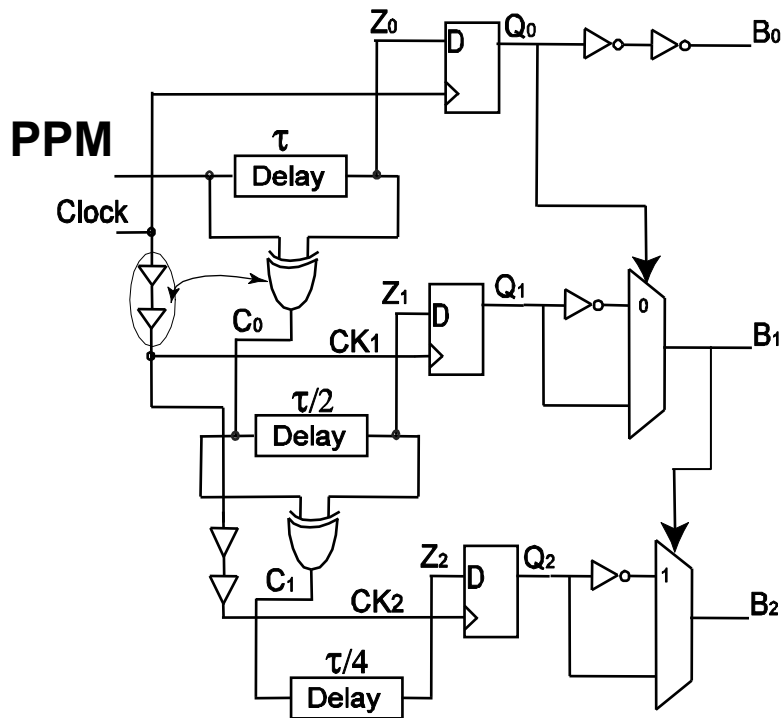
The TDC Architecture

- Hierarchical view of time processing

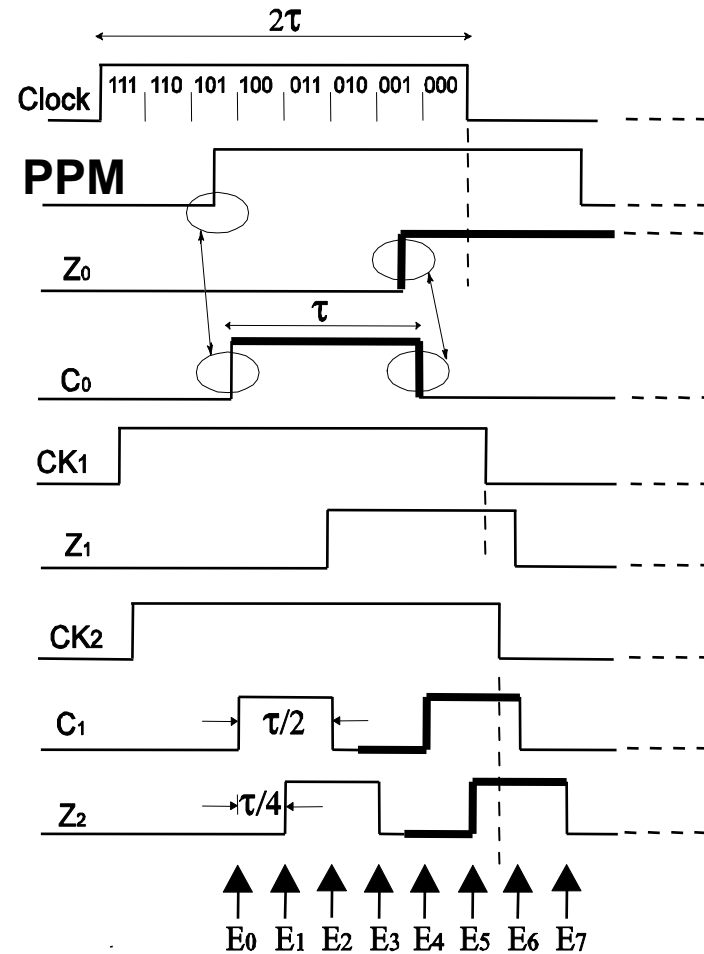


- # of Buffers = n
- Easier PVT control
- Single cycle latency

The TDC Design



Hierarchical TDC Design

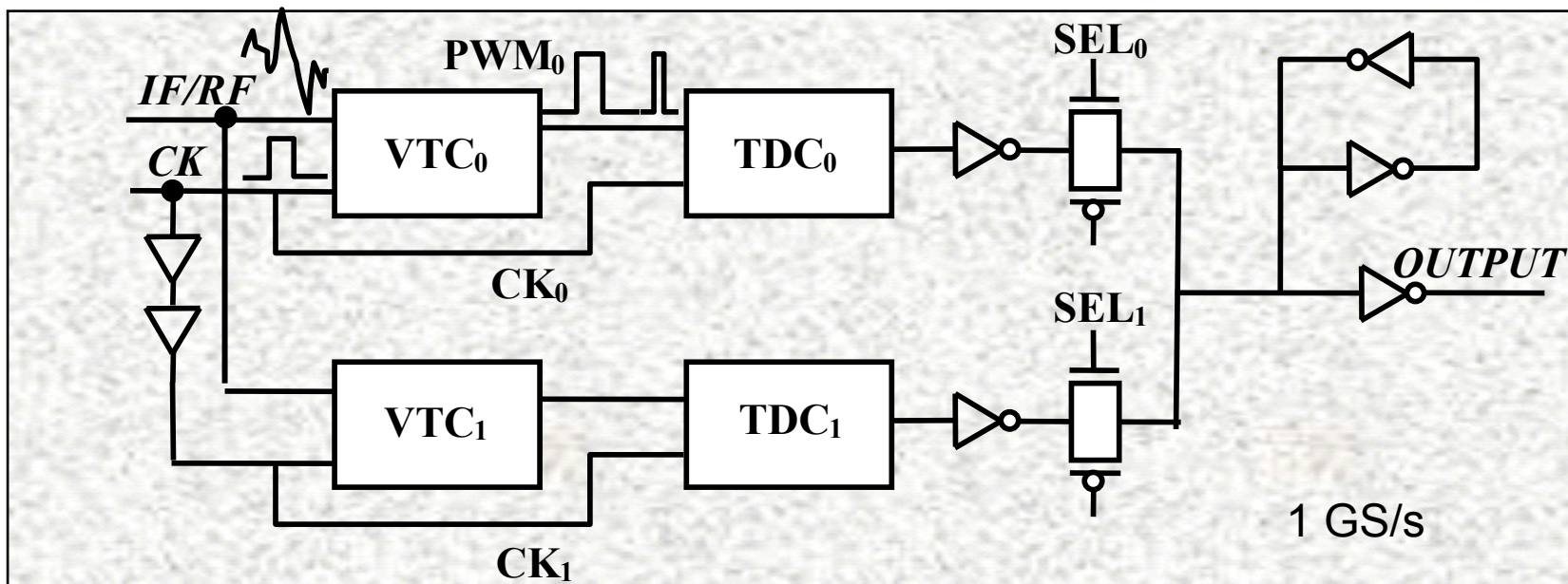


TDC Implementation

- This work focused on the highest resolution bits in a TDC system.
- A TDC for PET imaging implemented in the 130nm CMOS technology
 - Bit resolution: 6
 - Time resolution: 31 ps
 - Area: 0.15 sq. mm of active area
 - Power consumption*: 1 mW
 - Cycle latency*: 1

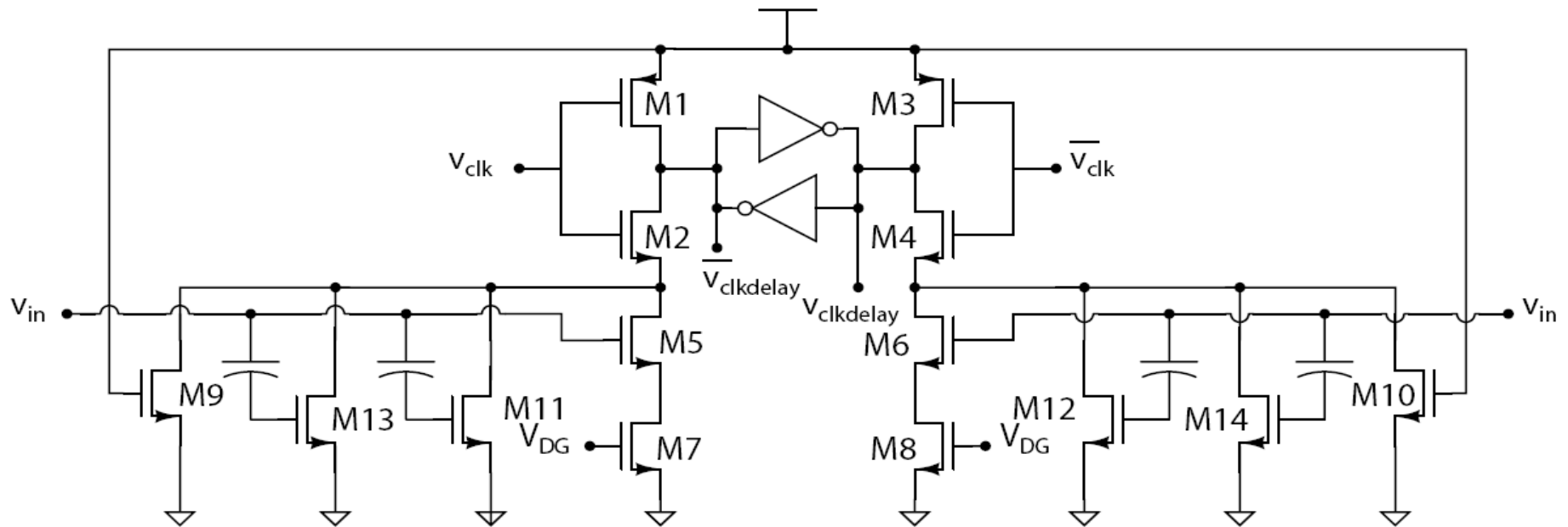
The ADC Architecture

- The focus is on low to medium resolution, high speed and low power design



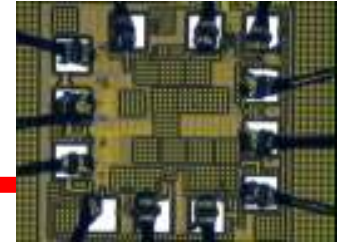
Two time-interleaved ADCs, each running at 500 MS/s

Voltage to Time Conversion



- Based on Voltage-Controlled delay
- No Sample-and-Hold required
- PVT and nonlinearity issues

ADC Implementation



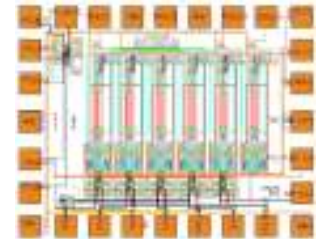
1 GS/s, 5-bit ADC built with two channels, each running at 500 MHz

- CMOS 130 nm process and 0.35 sq. mm. of area
- Measured SNDR: 27 dB at $f_{in} = 100$ MHz
- INL/DNL less than ± 0.6 LSB
- Measured power consumption: 4 mW
 - Two VTCs were used to achieve full delay range
 - No PVT Control
- US and Canadian patents filed for the TDC
- TDC architecture appeared in the IEEE Trans. On Nuclear Science, Vol. 54, No. 5, October 2007.

ADC Work in Progress

- 20 GS/s 2-bit ADC in 90nm CMOS

- 4 time-interleaved channels running at 5 GS/s



- Estimated power consumption: 200 mW

- 5 GS/s 3-bit ADC in 90nm CMOS

- New VTC and TDC architectures
- Highly tunable to mitigate process variations
- Estimated power consumption: 25 mW



Serial Data Links Status

- **3 GS/s serial link using multiple digital modulation techniques in the 90nm CMOS process**
 - First prototype simulation runs with a 500 Mhz clock (6:1 data encoding ratio)
 - Time-based building blocks and equalization/pre-emphasis circuits (no CDR)
 - Most circuit blocks run at 500 Mhz, not 3 Ghz as in traditional SerDes
 - New signaling technique guarantees zero differential jitter noise
 - PVT control using DLLs
 - Very low power (simulated) when compared to SerDes
- **FPGA prototyping underway**

Conclusions

- Time processing designs is an emerging research area with great potential
- It is redefining the design components for different applications
- The greatest potential is in pure digital design applications such as serial data links and low resolution, high speed DSP
- Time based designs scale well with process technology

References

- Holly Pekau, Abdel Yousif, and Jim Haslett, "[A CMOS Integrated Linear Voltage-to-Pulse-Delay-Time Converter for Time Based Analog-to-Digital Converters](#)", IEEE International Symposium on Circuits and Systems (ISCAS 2006), Kos, Greece, pp. 2373-2376. May 21-24, 2006.
- Abdel Yousif and Jim Halsett, "[A Fine Resolution TDC Architecture for Next Generation PET Imaging](#)", IEEE Transactions on Nuclear Science, VOL 54, NO 5, pp 1574-1582, October 2007.
- Abdel Yousif, Mostafa Rashdan, Jim Haslett, and Brent Maundy, "[A Low Power and High Speed PPM Design for UWB-ir Communications](#)", 21st Canadian Conference on Electrical and Computer Engineering, Ontario, Canada, May 2008.